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FIG. 1 PRIOR ART

FIG. 2 PRIOR ART

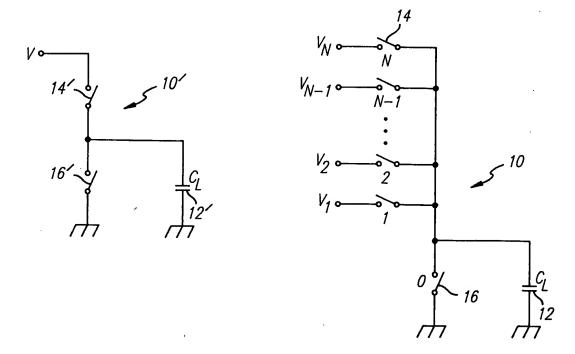
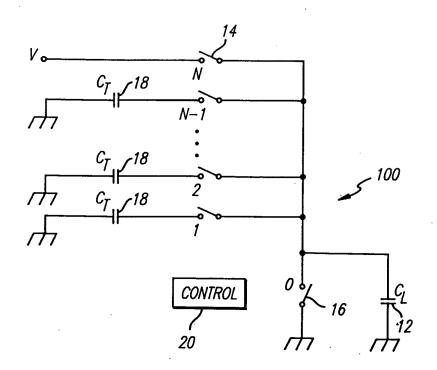


FIG. 3



VouT DRAF (SECH 2] OUTPUT LOGIC INPUT LOGIC LATCH \sim INPUT 5 FINITE STATE MACHINE 70 70 74 70 - X2072 20 2

FIG.

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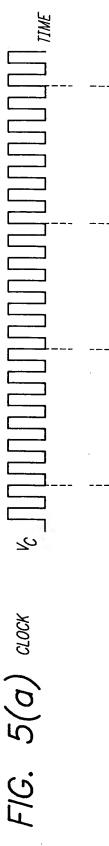


FIG. 5(b) INPUT
$$V_1$$
.

FIG. 5(c) SWITCH V_0 .



FIG.
$$5(e)$$
 SWITCH V_2

